Claims

[c1] An integrated circuit comprising:

a plurality of memory cells coupled in series to form a series group, the memory cells of a group are arranged in memory cell pairs, a memory cell pair of the group comprises;

a first memory cell having a first transistor having a gate and first and second diffusion regions and a first capacitor having first and second plates separated by a first capacitor dielectric;

a second memory cell having a second transistor having a gate and first and second diffusion regions and a second capacitor having first and second plates separated by second capacitor dielectric;

the second diffusion regions of the first and second transistors of the memory cell pair is a common second diffusion region;

the first and second capacitors are arranged in a stack in which the second plates of the capacitors is a common second plate;

the first plate of the first capacitor is coupled to the first diffusion region of the first transistor;

the first plate of the second capacitor is coupled to the first diffusion region of the second transistor; and

the common second plate is coupled to the common second diffusion region.

[c2] The integrated circuit of claim 1 wherein the memory cells are ferroelectric memory cells in which the capacitor dielectrics comprise a ferroelectric material.

[c3] The integrated circuit of claim 2 wherein the first plate of the first capacitor is coupled to the first diffusion region of the first transistor via a bottom first plate plug.

[c4] The integrated circuit of claim 2 wherein the common second plate is coupled to the common second diffusion via an active common second plate plug which is isolated from the first capacitor dielectric and first plate of the first capacitor.

[c5] The integrated circuit of claim 4 wherein the first plate of the first capacitor is coupled to the first diffusion region of the first transistor via a bottom first plate plug.

[c6] The integrated circuit of claim 1 wherein the first plate of the first capacitor is coupled to the first diffusion region of the first transistor via a bottom first plate plug.

[c7] The integrated circuit of claim 1 wherein the common second plate is coupled to the common second diffusion via an active common second plate plug which is isolated from the first capacitor dielectric and first plate of the first capacitor.

[c8] The integrated circuit of claim 6 wherein the first plate of the first capacitor is coupled to the first diffusion region of the first transistor via a bottom first plate plug.

[c9] The integrated circuit of claim 1 wherein first diffusion region of the second transistor of a first memory cell pair of adjacent memory cell pairs and the first diffusion region of the first transistor of a second memory cell pair of the adjacent memory cell pairs is a common first diffusion region of the adjacent memory cell pairs.

[c10] The integrated circuit of claim 9 wherein the first electrode of the second capacitor of the first adjacent memory cell pair is coupled to the first electrode of the first electrode of the first capacitor of the second adjacent memory cell pair and the common first diffusion region of the adjacent memory cell pairs.